PATENT ABSTRACTS OF JAPAN

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(54) **SOLID STATE IMAGE PICKUP DEVICE**

(57)Abstract:
PURPOSE: To provide the solid state image pickup device which can pick up an image
in a short storage period by simple structure, and start and end the storage of all pixels at
the same timing.
CONSTITUTION: The solid state image pickup device consists of a pixel group formed
by arranging pixels 10-11 to 10-mn composed of amplification type photodetecting
elements in matrix, plural row lines 11-1 to 11-m to which the gates of the pixels
arranged in an X direction in the pixel group are connected in common, plural column
lines 12-1 to 12-n to which the sources of the pixels arrayed in a Y direction in the pixel
group are connected in common, a storage part where storage cells (capacitor) 15-11 to
15-mn storing video signals of the respective pixels on the respective row lines are
arranged in matrix, a vertical scanning circuit 24 which applies a pixel read signal to the
row lines in order, and a horizontal scanning circuit 25 which outputs a driving signal for
outputting video signal currents stored in the respective storage cells in order.

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CLAIMS

[Claim(s)]
[Claim 1] The pixel group which has arranged the pixel which consists of a magnification
mold photo detector in the shape of a matrix, Two or more line Rhine which makes
common connection of the gate of each pixel arranged in the direction of X of said pixel
group, Two or more train Rhine which makes common connection of the source of each
pixel arranged in the direction of Y of said pixel group, The storage section by which two
or more storage cells which memorize the video signal of each pixel of each of said line
Rhine have been arranged in the shape of a matrix, The vertical-scanning circuit which
impresses a pixel read-out signal to said each line Rhine one by one, The solid state
camera characterized by are-recording-starting and ending the charge of each line Rhine
of a pixel group which possessed the horizontal scanning circuit which outputs the
driving signal which carries out the sequential output of the video-signal current
memorized by said each storage cell, and was prepared in image pick-up equipment to
the same timing in a storage region.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the solid state camera which changes an
optical image into an electrical signal using semiconductor technology.
[0002]
[Description of the Prior Art] Generally, there are solid state cameras, such as Charge
Modulation Device (Following CMD is called) using the magnification mold photo
detector which consists of a semiconductor device as a pixel.
[0003] The example of a configuration of the solid state camera which used this
conventional CMD as a pixel is shown in drawing 9 . This CMD arranges CMD 1-11
which constitutes each pixel, 1-12, --, 1-mn in the shape of a matrix, and impresses the
video electrical potential difference VDD (> 0) to each of that drain in common. the gate
terminal of the CMD group of each line arranged in the direction of X -- the source
terminal of line Rhine 2-1, 2-2, --, the CMD group of each train which connected with 2-
m in common, respectively, and was arranged in the direction of Y -- train Rhine 3-1, 3-2,
--, 3-n -- it connects in common, respectively. Train Rhine 3-1, 3-2, --, 3-n are connected

common to the video line 5 through the transistor 4-1 for train selection, 4-2, --, 4-n, respectively.

[0004] Said video line 5 is connected to the pre amplifier 6 of the current-electrical-potential-difference conversion mold with which the imaginary earth of the input edge was carried out, and the video signal of negative polarity is read to the outgoing end 7 of pre amplifier 6 by time series.

[0005] Moreover, line Rhine 2-1, 2-2, --, 2-m are connected to the vertical-scanning circuit 8, and a signal phiG1, phiG2, --phiGm are impressed, respectively. Direct continuation of the gate terminal of the transistor 4-1 for train selection, 4-2, --, 4-n is carried out to the horizontal scanning circuit 9, and it is constituted so that a signal phiS1, phiS2, --phiSn may be impressed, respectively. In addition, each CMD is formed on the same substrate and impresses VSUB (<0) to the substrate.

[0006] Drawing 10 is a signal waveform diagram for explaining actuation of the solid state camera of a configuration of having been shown in drawing 9 . Line Rhine 2-1 of this solid state camera, 2-2, --, the signal phiG1 impressed to 2-m, phiG2, --phiGm are read-out gate voltage VRD, the reset electrical potential difference VRS, the overflow electrical potential difference VOF, and the are recording electrical potential difference VINT. It becomes.

[0007] And it sets in a non-choosing line and they are the overflow electrical potential difference VOF and the level image shelf-life tH during the horizontal blanking interval tBL of a video signal. In inside, it is the are recording electrical potential difference VINT. It becomes. Moreover, it sets in a selection line and is the level image shelf-life tH. During the horizontal blanking interval tBL which reads to inside and follows gate voltage VRD and it, it becomes the reset electrical potential difference VRS.

[0008] Moreover, the transistor 4-1 for train selection, 4-2, --, the signal phiS1 impressed to the gate terminal of 4-n, phiS2, --phiSn By train Rhine 3-1, 3-2, --, the signal for choosing 3-n, the low is set up so that it may become the transistor 4-1 for train selection, 4-2, --, electrical-potential-difference value on which 4-n is turned off and the high level turns on the transistor for train selection.

[0009] In the solid state camera of the above configuration, by a signal's phiG's1 reading and becoming an electrical potential difference, CMD of the 1st line is chosen, and continuously, a signal phiS1, phiS2, --, when phiSn turns on, 1-11, 1-12, --, the signal current from one to 1 n are read via a video line one by one. Furthermore, a signal phiG1, phiG2, --, phiGm are made into a read-out electrical potential difference one by one, whenever [the], a signal phiS1, phiS2, --, phiSn serve as ON, and the signal of all pixels is read one by one.

[0010]

[Problem(s) to be Solved by the Invention] However, in the conventional solid state camera mentioned above, since read-out of a signal is performed by sequential scanning, the timing of are recording initiation and termination will differ for every pixel.

[0011] Although it is convenient that such timing differs for an application which picturizes an animation and is reproduced as it is, trouble appears in applications, such as image measurement, for example. That is, in order to measure the body which moves at high speed, it is a short exposure period and it is necessary to obtain the image of the same time of day but, and in the conventional solid state camera, since the read time which became settled in order to obtain one image is needed, one perfect image cannot be

obtained by the short exposure period not more than it.

[0012] As a solid state camera which solves this fault, there is a solid state camera which transmits the charge accumulated for every pixel to an amplifier so that it may be proposed by JP,61-84058,A. However, in said solid state camera, since the structure of a pixel becomes complicated and area also becomes large, there is a fault that high integration is difficult.

[0013] Then, this invention aims to let all pixels offer the solid state camera in which are recording initiation and termination are possible to this timing that it can picturize in a short are recording period with easy structure.

[0014]

[Means for Solving the Problem] The pixel group which has arranged the pixel which consists of a magnification mold photo detector in the shape of a matrix in order that this invention may attain the above-mentioned purpose, Two or more line Rhine which makes common connection of the gate of each pixel arranged in the direction of X of said pixel group, Two or more train Rhine which makes common connection of the source of each pixel arranged in the direction of Y of said pixel group, The storage section by which two or more storage cells which memorize the video signal of each pixel of each of said line Rhine have been arranged in the shape of a matrix, The vertical-scanning circuit which impresses a pixel read-out signal to said each line Rhine one by one, It consists of horizontal scanning circuits which output the driving signal which carries out the sequential output of the video-signal current memorized by said each storage cell, and the solid state camera which ends [which is ended and are-recording-begins] the charge of each line Rhine of a pixel group prepared in image pick-up equipment to the same timing in a storage region is offered.

[0015]

[Function] By preparing the storage region which accumulates the charge of each line Rhine of a light sensing portion in image pick-up equipment, and transmitting the accumulated charge through train Rhine, to the timing that each pixel is almost the same, it is are-recording-started and the solid state camera of the above configurations is ended.

[0016]

[Example] Hereafter, the example of this invention is explained to a detail with reference to a drawing.

[0017] The configuration of the solid state camera as the 1st example by this invention is shown in <u>drawing 1</u> , and it explains to it. CMD 10-11 which constitutes each pixel in this solid state camera, 10-12, --, 10-mn are arranged in the shape of a matrix. The video electrical potential difference VDD (> 0) is impressed to each drain of CMD in common. The source terminal of the CMD group of each [line Rhine 11-1, 11-2, --, / that were connected to 11-m in common, respectively, and were arranged in the direction of Y] train is connected to train Rhine 12-1, 12-2, --, 12-n for the gate terminal of the CMD group of each line arranged in the direction of X in common, respectively. Train Rhine 12-1, 12-2, --, 12-n are connected to are recording train Rhine 14-1, 14-2, --, 14-n through the transfer transistor 13-1, 13-2, --, 13-n, respectively.

[0018] It connects with 14-n through the cel selection transistor 16-11, 16-12, --, 16-mn, and each are recording train Rhine 14-1, 14-2, --, the capacitor 15-11 arranged in the shape of a matrix, 15-12, --, 15-mn form the are recording section in it. The gate of the cel selection transistor 16-11, 16-12, --, 16-mn is connected to are recording line Rhine

17-1, 17-2, and 17-m.

[0019] And the end of are recording train Rhine 14-1, 14-2, --, 14-n is connected also to the drain of the train read-out transistor 18-1, 18-2, --, 18-n through the are recording selection transistor 19-1, 19-2, --, 19-n while connecting with the gate of the train read-out transistor 18-1, 18-2, --, 18-n. The drain of said train read-out transistor 18-1, 18-2, --, 18-n is further connected common to the video line 21 through the train selection transistor 20-1, 20-2, --, 20-n. The video line 21 is connected to the pre amplifier 22 of the current-electrical-potential-difference conversion mold with which the imaginary earth of the input was carried out, and a video signal is read to the outgoing end 23 of said pre amplifier 22 by time series.

[0020] Moreover, line Rhine 11-1, 11-2, --, 11-m are connected to the vertical-scanning circuit 24, and a signal phiG1, phiG2, --, phiGm are impressed, respectively. Moreover, similarly are recording line Rhine 17-1, 17-2, and 17-m are connected to the vertical-scanning circuit 24, and signal phiC1, phiC2, --, phiCm are impressed, respectively. In the gate of the transfer transistor 13-1, 13-2, --, 13-n, it is signal phiT. It is impressed and is signal phiH in the gate of the are recording selection transistor 19-1, 19-2, --, 19-n. It is impressed.

[0021] And direct continuation of the gate terminal of the train selection transistor 20-1, 20-2, --, 20-n is carried out to the horizontal scanning circuit 25, and it is constituted so that a signal phiS1, phiS2, --, phiSn may be impressed, respectively. Furthermore, are recording train Rhine 14-1, 14-2, --, 14-n are connected to the reset transistor 26-1, 26-2, --, Rhine grounded through 26-n. Signal phiRS is impressed to the gate of the reset transistor 26-1, 26-2, --, 26-n in common from the vertical-scanning circuit 24. Next, example actuation is explained to <u>drawing 2</u> for the signal waveform diagram of each point of the solid state camera of a configuration of having been shown in <u>drawing 1</u>.

[0022] Here, line Rhine 11-1, 11-2, --, the signal phiG1 impressed to 11-m, phiG2, --, phiGm are read-out gate voltage VRD, the reset electrical potential difference VRS, the overflow electrical potential difference VOF, and the are recording electrical potential difference VINT. It becomes. usually, are recording electrical potential difference VINT it is -- horizontal blanking interval tHBL of a video signal Inside serves as the overflow electrical potential difference VOF. Vertical-retrace-line period tVBL Inside is read for every selection line, takes gate voltage VRD, and serves as the reset electrical potential difference VRS at all line coincidence following on it.

[0023] first -- phiG to all line Rhine 11-1, 11-2, --, 11-m All CMD(s) are reset to becoming a reset electrical potential difference at coincidence. Then, a line Rhine signal is the are recording electrical potential difference VINT. It becomes and are recording of a photoelectric load is started. In the pixel in which light carried out incidence, an electron hole is accumulated in the bottom of the gate of CMD among the generated electron-hole pairs. For this reason, the potential under the gate of CMD rises according to the quantity of light.

[0024] The signal of each pixel is read after the predetermined storage time. Signal phiT and phiH It is referred to as "Hi", and phiG1 reads first and an electrical potential difference and phiC1 are set to "Hi." Thereby, CMD 10-11, 10-12, --, the signal current according to the stored charge which ten to 1 n is chosen and is each pixel arise, and a capacitor 15-11, 15-12, --, 15 to 1 n are charged via train Rhine 12-1, 12-2, --, 12-n and are recording train Rhine 14-1, 14-2, --, 14-n, respectively.

[0025] At this time, the are recording selection transistor 19-1, 19-2, --, since 19-n turns on, a current arises also in the train read-out transistor 18-1, 18-2, --, 18-n. And when the current of CMD 10-11 and the current of the train read-out transistor 18-1 become equal, the charge to a capacitor 15-11 stops, and the potential which gives a current equal to a pixel signal is memorized.

[0026] Similarly, the signal of CMD 10-12, 10-13, --, ten to 1 n is accumulated in a capacitor 15-12, 15-13, --, 15 to 1 n at coincidence. Then, phiG2 reads, an electrical potential difference and phiC2 serve as "Hi", and the signal of CMD 10-21, 10-22, --, ten to 2 n is accumulated in a capacitor 15-21, 15-22, --, 15 to 2 n by the same actuation at coincidence.

[0027] Hereafter, while phiG3 and phiC3, phiG4 and phiC4, --, phi Gm-phi Cm are turned on, the 3rd line, the 4th line, --, the pixel signal of the m-th line are transmitted to the capacitor of the are recording section.

[0028] And phiH after a transfer is completed It is turned off and a signal is read from the are recording section one by one. phiC1 serves as ON first and the gate of the train read-out transistor 18-1, 18-2, --, 18-n is connected to a capacitor 15-1, 15-2, --, 15-n, respectively. The signal current of a pixel 10-11 and an equal current are absorbed by the train read-out transistor 18-1 because a signal phiS1 serves as "Hi" here. Via the video line 21, this current is transformed into an electrical potential difference by pre amplifier 22, and serves as a signal of a pixel 10-11. Then, the signal current of a pixel 10-12 is absorbed by the train read-out transistor 18-2 because a signal phiS2 serves as "Hi."

[0029] Hereafter, signal read-out of the 1st line is performed because phiSn serves as [phiS3, phiS4, --,] "Hi." Then, the 2nd line is chosen because phiC2 serves as "Hi", and the signal of a pixel 10-21, 10-22, --, ten to 2 n is read one by one because phiSn serves as [phiS1, phiS2, --,] "Hi." Hereafter, while phiC3, phiC4, --, phiCm are turned on, the 3rd line, the 4th line, --, the pixel signal of the m-th line are read one by one. In addition, at the last of read-out of each line, the reset transistor 26 serves as ON by phiRS, and are recording train Rhine 14-1, 14-2, --, the capacitor of the line which 14-n is made into touch-down potential, and is chosen reset.

[0030] As mentioned above, in the solid state camera of this invention, the signal transfer to the are recording section from Pixel CMD bundles up within a perpendicular blanking period, and is performed. Since the transfer period for every line can also be shortened very much, it can consider that the timing of the are recording initiation and termination which is each pixel is almost the same, and, therefore, a static image can be picturized in a short are recording period.

[0031] Next, the configuration of the solid state camera as the 2nd example by this invention is shown in <u>drawing 3</u> , and it explains to it. Here, the same reference mark is given to a member equivalent to the configuration member shown in <u>drawing 1</u> by the configuration member of the 2nd example, and the explanation is omitted. This solid state camera is equipped with the pixel CMD 10-11 arranged in the shape of a matrix, 10-12, --, 10-mn and line Rhine 11-1 which connects the gate terminal of the CMD group of each line arranged in the direction of X, 11-2, --, 11-m and train Rhine 12-1 which connects the source terminal of the CMD group of each train arranged in the direction of Y, 12-2, --, 12-n. These train Rhine 12-1, 12-2, --, 12-n are connected to are recording train Rhine 14-1, 14-2, --, 14-n through the transfer transistor 13-1, 13-2, --, 13-n, respectively.

[0032] And it connects with 14-n through the cel selection transistor 16-11, 16-12, --, 16-

Ln, and each are recording train Rhine 14-1, 14-2, --, the capacitor 15-11 arranged in the shape of a matrix, 15-12, --, 15-Ln form the are recording section in it. The gate of the cel selection transistor 16-11, 16-12, --, 16-Ln is connected to are recording line Rhine 17-1, 17-2, --, 17-l. In this example, more line counts l of the are recording section than the line count m of a pixel matrix are formed.

[0033] Moreover, the end of said are recording train Rhine 14-1, 14-2, --, 14-n is connected also to the drain of the train read-out transistor 18-1, 18-2, --, 18-n through the are recording selection transistor 19-1, 19-2, --, 19-n while connecting with the gate of the train read-out transistor 18-1, 18-2, --, 18-n. The drain of the train read-out transistor 18-1, 18-2, --, 18-n is further connected common to the video line 21 through the train selection transistor 20-1, 20-2, and 20-n.

[0034] Next, the video line 21 is connected to the pre amplifier 22 of the current-electrical-potential-difference conversion mold with which the imaginary earth of the input was carried out, and a video signal is read to the outgoing end 23 of this pre amplifier 22 by time series.

[0035] Moreover, line Rhine 11-1, 11-2, --, 11-m are connected to the vertical-scanning circuit 24, and a signal phiG1, phiG2, --, phiGm are impressed, respectively. Moreover, are recording line Rhine 17-1, 17-2, and 17-l are connected to a selector 27, and signal phiC1, phiC2, --, phiCm are impressed to m lines as which it was chosen in l lines, respectively. Furthermore, the selector 27 is connected to the vertical-scanning circuit 24 and ROM (read-only memory)28. In the gate of said transfer transistor 13-1, 13-2, --, 13-n, it is signal phiT. It is impressed and is signal phiH in the gate of the are recording selection transistor 19-1, 19-2, --, 19-n. It is impressed. Direct continuation of the gate terminal of said train selection transistor 20-1, 20-2, --, 20-n is carried out to the horizontal scanning circuit 25, and it is constituted so that a signal phiS1, phiS2, --, phiSn may be impressed, respectively. Furthermore, are recording train Rhine 14-1, 14-2, --, 14-n are connected to the reset transistor 26-1, 26-2, --, Rhine grounded through 26-m.

[0036] The solid state camera of this 2nd example investigates the existence of the defect of the are recording section in the phase where the solid state camera was manufactured, and is to replace with a spare are recording line to a line with a defect. For this reason, the chip which has some defects in the are recording section also becomes usable. In advance of actuation of a solid state camera, the capacitor of the are recording section and actuation of a cel selection transistor are checked by the semi-conductor circuit tester etc. When there is a malfunction by the crystal defect or leak, the line is recorded, and it is replaced with a reserve line. This replacement information is recorded on ROM28 of the vertical-scanning section.

[0037] After the above-mentioned information setup is made, actuation of this solid state camera is fundamentally the same as that of the 1st example. All line Rhine 11-1, 11-2, --, phiG to 11-m All CMD(s) are reset by becoming a reset electrical potential difference at coincidence. Then, a line Rhine signal is the are recording electrical potential difference VINT. It becomes and a photoelectrical load is accumulated. The signal of each pixel is read after the predetermined storage time. Signal phiT and phiH It is made "Hi," and phiG1 reads first and an electrical potential difference and phiC1 are set to "Hi." The 1st line of a picture element part is chosen by this, the signal current according to the stored charge which is each pixel arises, and the capacitor of the are recording line (line replaced when the 1st line did not have a defect and there were the 1st line and a defect)

which corresponds via train Rhine and are recording train Rhine is charged. When the current of CMD and the current of a train read-out transistor become equal in each train, the potential which gives a current with the charge equal to a stop and a pixel signal to a capacitor is memorized. Hereafter, while phiG2 and phiC2, phiG3 and phiC3, --, phi Gm-phi Cm are turned on, the 3rd line, the 4th line, --, the pixel signal of the m-th line are transmitted to the capacitor of the are recording section. As mentioned above, with the solid state camera of the 2nd example, the chip which has some defects in the are recording section also becomes usable, the yield improves and cost becomes cheap.

[0038] Next, the configuration of the solid state camera as the 3rd example by this invention is shown in drawing 4 , and it explains to it. Here, the same reference mark is given to a member equivalent to the configuration member shown in drawing 1 by the configuration member of the 3rd example, and the explanation is omitted.

[0039] This solid state camera is equipped with the pixel CMD 10-11 arranged in the shape of a matrix, 10-12, --, 10-mn and line Rhine 11-1 which connects the gate terminal of the CMD group of each line arranged in the direction of X, 11-2, --, 11-m and train Rhine 12-1 which connects the source terminal of the CMD group of each train arranged in the direction of Y, 12-2, --, 12-n. Train Rhine 12-1, 12-2, --, 12-n are connected to are recording train Rhine 14-1, 14-2, --, 14-n through the transfer transistor 13-1, 13-2, --, 13-n, respectively.

[0040] It connects with 14-n through the cel selection transistor 16-11, 16-12, --, 16-mn, and each are recording train Rhine 14-1, 14-2, --, the capacitor 15-11 arranged in the shape of a matrix, 15-12, --, 15-mn form the are recording section in it. The gate of the cel selection transistor 16-11, 16-12, --, 16-mn is connected to are recording line Rhine 17-1, 17-2, --, 17-m.

[0041] The end of said are recording line Rhine 14-1, 14-2, --, 14-n is connected also to the drain of the train read-out transistor 18-1, 18-2, --, 18-n through the are recording selection transistor 19-1, 19-2, --, 19-n while connecting with the gate of the train read-out transistor 18-1, 18-2, --, 18-n. The drain of said train read-out transistor 18-1, 18-2, --, 18-n is further connected common to the video line 21 through the train selection transistor 20-1, 20-2, --, 20-n. This video line 21 is connected to the pre amplifier 22 of the current-electrical-potential-difference conversion mold with which the imaginary earth of the input was carried out, and a video signal is read to the outgoing end 23 of pre amplifier 22 by time series.

[0042] Moreover, line Rhine 11-1, 11-2, --, 11-m are connected to the vertical-scanning circuit 24, and a signal phiG1, phiG2, --, phiGm are impressed, respectively. Moreover, signal phiC1, phiC2, --, phiCm are impressed to are recording line Rhine 17-1, 17-2, and 17-l, respectively. In the gate of the transfer transistor 13-1, 13-2, --, 13-n, signal phiT is signal phiH again to the gate of the are recording selection transistor 19-1, 19-2, --, 19-n. It is impressed, respectively. Direct continuation of the gate terminal of the train selection transistor 20-1, 20-2, --, 20-n is carried out to the horizontal scanning circuit 25, and it is constituted so that a signal phiS1, phiS2, --, phiSn may be impressed, respectively. Furthermore, are recording train Rhine 14-1, 14-2, --, 14-n are connected to the reset transistor 26-1, 26-2, --, Rhine grounded through 26-n.

[0043] The current store circuit 30-1, 30-2, --, 30-n are connected to said train Rhine 12-1, 12-2, --, 12-n. In each current store circuit, they are a signal phiR1, phiR2, and phiT from the vertical-scanning circuit 24. It is impressed. The configuration of a current store

circuit is shown in <u>drawing 5</u> here.

[0044] As for this current store circuit, the transistor 31 by which the drain was connected to train Rhine 12, and a transistor 32 constitute current Miller circuit. The gate of a transistor 31 and a transistor 32 interconnects, and the capacitor 35 is connected through the transistor 34. The drain of said transistor 32 is connected to the drain of the P channel transistor 36 through a transistor 40.

[0045] The drain of said P channel transistor 36 is connected to the capacitor 38 through the transistor 37. The capacitor 38 is connected between the gate of the P channel transistor 36, and the source. A signal phiR1 is impressed to the gate of a transistor 37, and a signal phiR2 is impressed to the gate of a transistor 34.

[0046] Furthermore, the drain of said transistor 31 is connected to the drain of a transistor 36 through the transistor 39 at the gate of a transistor 31 through the transistor 33, respectively. In the gate of said transistor 39, it is signal phiT. Moreover, phiT outputted to the gate of a transistor 33 and a transistor 40 from an inverter 41 A reversal signal is impressed, respectively.

[0047] The solid state camera of this 3rd example records the information which deducted the output level at the time of the dark of each pixel from signal level on the are recording section. For this reason, dispersion in the black level of each pixel can be canceled, and the output with which the fixed pattern noise was reduced can be obtained. Next, with reference to the signal waveform diagram of <u>drawing 6</u> , actuation of the solid state camera constituted in this way is explained.

[0048] First, the signal transfer to the are recording section from a picture element part is the perpendicular blanking period tVBL like a last example. It is carried out. The impression pulse phiG1 to line Rhine 11-1 is read at the time of transfer initiation, and serves as an electrical potential difference VRD, and a signal phiR1 serves as "Hi" at coincidence at this time. For this reason, the signal current read from each pixel of the 1st line is reversed in the current Miller circuit of the current store circuit 30, and while a current equal to the P channel transistor 36 arises, the gate potential at this time is memorized by the capacitor 38. Then, phiG1 becomes the reset electrical potential difference VRS, and the stored charge of each pixel is reset.

[0049] While further phiG1 becomes the read-out electrical potential difference VRD again and the signal of the black level of each pixel is read, when phiR2 is turned on, the signal current of black level arises to a transistor 31, and this gate potential is memorized by the capacitor 35.

[0050] Next phiC1 and phiT And phiH It is set to "Hi" and the signal transfer to the are recording section from the current store circuit 30 is performed (phiG1 becomes the are recording electrical potential difference VINT at this time, and the signal from a pixel is not read). The signal current at the time of ** of a pixel arises to the P channel transistor 36 of said current store circuit 30, and the signal current at the time of dark arises to a transistor 31. While the current equivalent to both difference reads via train Rhine 12 and are recording train Rhine 14 and arises to a transistor 18, the gate potential which gives this current is memorized by the capacitor 15 of the 1st line of the are recording section. The above actuation is succeedingly performed also to the 2nd line and 3rd line --, and the pixel signal with which black level was canceled is memorized by the are recording section.

[0051] After this, like each example mentioned above, sequential impression of the

potential memorized by the capacitor of the are recording section is carried out for every line, and a signal is read to the gate of a read-out transistor through the video line 21 and pre amplifier 22.

[0052] In this 3rd example, the information which deducted the output level at the time of the dark of each pixel from signal level can be recorded on the are recording section, and the output with which dispersion in the black level of each pixel was canceled, and the fixed pattern noise was reduced can be obtained.

[0053] Next, the configuration of the solid state camera of the 4th example by this invention is shown in drawing 7 , and it explains to it. This example unifies functionally a solid state camera and the processing to the picturized image.

[0054] This solid state camera is equipped with the pixel CMD 10-11 arranged in the shape of a matrix, 10-12, --, 10-mn and line Rhine 11-1 which connects the gate terminal of the CMD group of each train arranged in the direction of X, 11-2, --, 11-m and train Rhine 12-1 which connects the source terminal of the CMD group of each train arranged in the direction of Y, 12-2, --, 12-n. Train Rhine 12-1, 12-2, --, 12-n are connected to are recording train Rhine 14-1, 14-2, --, 14-n, respectively. Each are recording train Rhine 14-1, 14-2, --, 14-n and are recording line Rhine 17-1, 17-2, -- and the processing element 42-11 arranged in the shape of a matrix, 42-12, --, 42-mn are connected to 17-m, and the are recording processing section is formed in it.

[0055] The configuration of a processing element is shown in drawing 8 here. In this processing element, the input from are recording train Rhine 14 is memorized through the selection transistor 16 in the signal holding circuit 44. The gate of said selection transistor 16 is connected to are recording line Rhine 17, and the signal holding circuit 44 is connected to the processor 46 through the quantization circuit 45.

[0056] Thus, actuation of the constituted processing element is explained. The sequential transfer of the signal charge accumulated by each pixel is carried out for every line from a light sensing portion to the are recording section. That is, current-electrical-potential-difference conversion of the current of Pixel CMD is carried out in the signal holding circuit 44 of the processing element chosen by the selection transistor 16, and potential is held at a capacitor. This signal is changed into digital value, such as binary-izing or 2 bits, and 4 etc. bits, in the quantization circuit 45. The digitized signal is inputted into a processor 46 and it processes using the signal from the quantization circuit 45, and the signal transmitted from a nearby processor in a processor 46.

[0057] As processing here, there are an edge extract, thinning, animal object detection, locus drawing, etc., and it performs by the instruction given from a control circuit. A processing result is outputted to juxtaposition from each processor.

[0058] the image of the body which the processing to this solid state camera and an image is unified functionally, for example, is suitable for the solid state camera of the 4th example for applications, such as image measurement, as mentioned above, and moves at high speed -- all **** -- it is possible to picturize to the almost same timing and to perform processing for measurement. it explained above -- as -- the image pick-up in an are recording period short with structure with the easy solid state camera of this invention -- it can do -- and all **** -- are recording initiation and closing can be performed to the almost same timing. Moreover, as for this invention, it is needless to say for the deformation and application various in the range which are not limited to the example mentioned above and do not deviate from the summary of invention to others to be

possible.

[0059]

[Effect of the Invention] As explained in full detail above, according to this invention, all pixels can offer the solid state camera in which are recording initiation and termination are possible to this timing that it can picturize in a short are recording period with easy structure.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing the configuration of the solid state camera as the 1st example by this invention.

[Drawing 2] It is the signal waveform diagram of each point of the solid state camera of a configuration of having been shown in drawing 1 .

[Drawing 3] It is drawing showing the configuration of the solid state camera as the 2nd example by this invention.

[Drawing 4] It is drawing showing the configuration of the solid state camera as the 3rd example by this invention.

[Drawing 5] It is drawing showing the configuration of the current store circuit of the solid state camera of the 3rd example.

[Drawing 6] It is a signal waveform diagram for explaining actuation of the solid state camera of the 3rd example.

[Drawing 7] It is drawing showing the configuration of the solid state camera as the 4th example by this invention.

[Drawing 8] It is drawing showing the configuration of the processing element of the solid state camera of the 4th example.

[Drawing 9] Drawing 9 is drawing showing the example of a configuration of the solid state camera by the conventional CMD.

[Drawing 10] Drawing 10 is a signal waveform diagram for explaining actuation of the solid state camera of a configuration of having been shown in drawing 9 .

[Description of Notations]

10-11 - 10-mn--Charge Modulation Device (CMD), 11-1 - 11-m -- Line Rhine, 12-1 - 12-n -- Train Rhine, 13-1 - 13-n -- Transfer transistor, 14-1 - 14-n -- Are recording train Rhine, 15-11-15-mn -- Capacitor, 16-11-16-mn -- A cel selection transistor, 17-1 - 17-m -- Are recording line Rhine, 18-1 - 18-n [-- A video line, 22 / -- Pre amplifier, 23 / -- An outgoing end, 24 / -- A vertical-scanning circuit, 26-1 - 26-n / -- Reset transistor.] -- A train read-out transistor, 19-1 - 19-n -- An are recording selection transistor, 20-1 - 20-n -- A train selection transistor, 21